REMARKS

This Amendment is responsive to the Office Action dated May 12, 2004. Applicant has amended claims 1-3, 9, 14-16, 19, 21, 22, 25, 28, 29, and 32, and canceled claims 5 and 30. Claims 1-4, 6-29, 31 and 32 are pending in the present application.

Allowable Subject Matter

In the Office Action, the Examiner allowed claim 20 and indicated that claims 9, 10, 16, 25, 26, and 32 would be allowable if rewritten in independent form.

Amendments

In this Amendment, Applicant has amended the claims to more appropriately define the invention.

Amended claims 1, 21, and 28 now specify that the first propagation delay is a "clock-to-Q" propagation delay. Accordingly, claims 5 and 30, which formerly recited that limitation, have been canceled.

Applicant has rewritten claim 2 in independent form, including all of the limitations of original base claim 1, and corrected minor informalities noted by the Examiner.

Amended claim 3 now properly refers to "current sinking," rather than "current signal," characteristics of the flip-flop.

Amended claim 9 has been rewritten in independent form to include all of the limitations of original base claim 1, and should be allowable, along with dependent claim 10.

Applicant has amended claim 14 to specify that the delay matching circuit matches a propagation delay introduced to a divided clock signal by a flip-flop in a clock divider, and that the transmission gates, inputs and output substantially mimic characteristics of a slave transmission gate, master output driver, and output driver, respectively, the flip-flop in the clock divider.

Amended claim 15 addresses an antecedent issue with respect to the flip-flop.

Applicant has rewritten claim 16 in independent form, including all of the limitations of original base claim 14. Claim 16 should now be allowable.

Amended claims 18 and 19 address an antecedent issue with respect to the propagation delay and clock signal, respectively.

Applicant has rewritten claim 22 in independent form to include the limitations of original base claim 21, and rewritten claim 25 in independent form to include the limitations of original base claims 21 and 23.

Amended claim 29 addresses an antecedent issue with respect to the "flip-flop."

Applicant has rewritten claim 32 in independent form to include the limitations of original base claims 28 and 31.

Applicant respectfully submit that the amended claims satisfy the requirements of 35 U.S.C. § 112, second paragraph. In addition, the minor amendments to claims 2 and 14 adequately address the objections raised by the Examiner. Accordingly, Applicant respectfully requests withdrawal of the objections to claims 2 and 14, and the rejection of claims 18 and 19 under 25 U.S.C. 112, second paragraph.

Claim Rejection Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1, 3, 5, 13, 28 and 30 under 35 U.S.C. 102(b) as being anticipated by JP Patent No. JP409046189A to Oosera et al., and rejected claims 14, 15, 17, and 21 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,477,592 to Chen et al.

Claims 5 and 30 have been canceled. Claims 1 and 28 incorporate the limitations previously set forth in claims 5 and 30, respectively.

Applicant respectfully traverses the rejections to the extent such rejections may be considered applicable to amended claims 1, 3, 13, and 28. As discussed below, the applied references fail to disclose all of the features set forth in the claims, and provide no teaching that would have suggested the desirability of modification to include such features.

Claims 1, 3, 5, 13, 28 and 30 - Oosera et al.

From Applicant's inspection of both JP409046189A and counterpart U.S. Patent No. 5,767,720 (collectively Oosera et al.), it is clear that Oosera et al. fails to disclose all of the features required by claims 1, 3, 13, and 28.

In his analysis, the Examiner stated that Oosera et al. discloses, in FIG. 1, a clock distribution circuit comprising a clock source 10 to generate a clock signal, a clock divider 11 including a D flip-flop that introduces a first propagation delay into the divided clock signal. The

Examiner further stated that Oosera et al. provides a delay matching circuit 12 that introduces a second propagation delay substantially matching the first propagation delay.

Contrary to the requirements of amended claims 1, 3 and 13, however, Oosera et al. fails to disclose a delay matching circuit configured to introduce a second propagation delay to the clock signal that substantially matches the clock-to-Q propagation delay introduced in the divided clock signal by the flip-flop in the clock divider.

Similarly, Oosera et al. neither discloses nor suggests a method comprising introducing, with a delay matching circuit, a second propagation delay to the clock signal that substantially matches the clock-to-Q propagation delay introduced in the divided clock signal by the flip-flop, wherein the delay matching circuit substantially mimics delay characteristics of the flip-flop, as set forth in amended claim 28.

Oosera et al. does not provide circuitry for introducing a propagation delay that substantially matches a clock-to-Q propagation delay of the flip-flop in clock divider 11. Instead, Oosera et al. describes a delay circuit 12 with a flip-flop that appears to match a reset-to-Q delay in flip-flop 11.

For example, as shown in FIG. 1 of Oosera et al., clock source 10 is coupled in common to both the clock input (CP) and the set/reset input (CD) of the flip-flop in delay circuit 12. Consequently, the propagation delay produced by the flip-flop in delay circuit 12 would not substantially match the clock-to-Q delay of the flip-flop in clock divider 11, but rather the reset-to-Q delay.

The reset-to-Q delay is typically different from the clock-to-Q delay in a flip-flop. Therefore, although Oosera et al. indicates that the signal delay produced by delay circuit 12 is equal to the delay produced the frequency divider circuit 11, the result may be quite different in operation. Hence, in failing to substantially match the clock-to-Q delay, the Oosera et al. circuit fails to anticipate the claimed invention.

Moreover, with respect to claim 13, Oosera et al. makes no mention of an asynchronous reset feature in delay circuit 12 that mimics operation of an asynchronous reset feature in frequency divider circuit 11. As shown in FIG. 1, CD input of the delay circuit 12 is coupled in common to the clock input of the flip-flop. Therefore, delay circuit 12 cannot be asynchronously reset like frequency divider circuit 11.

In view of the differences described above, the Oosera et al. reference fails to anticipate claims 1, 3, 13, and 28, as amended. For at least these reasons, Oosera et al. would not support a prima facie case of anticipation with respect to claims 1, 3, 13 and 28, or any claims dependent on those claims.

Claims 14, 15, 17, and 21 – Chen et al.

With reference to FIG. 7, the Examiner characterized Chen et al. as disclosing a delay matching circuit having a multiplexer coupled to a clock source CLK2, transmission gates 66, 68, 70, 72 and 74, 76, 78, 80 to substantially mimic characteristics of a slave transmission gate in a flip-flop, inputs D, Db coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of the output driver of the flip-flop.

Contrary to the requirements of amended claims 14, 15, 17 and 21, however, Chen et al. does not describe a circuit for matching a propagation delay introduced to a divided clock signal by a flip-flop in a clock divider. Rather, Chen et al. describes the circuitry of FIG. 7 as merely a data encoder 54 for transferring data out of a semiconductor chip. Hence, Chen et al. makes no mention of a clock divider, a flip-flop in a clock divider, or any desire to substantially mimic the characteristics of particular features within the flip-flop in the clock divider.

For example, Chen et al. fails to contemplate the configuration of transmission gates 66, 68, 70, 72 and 74, 76, 78, 80 to substantially mimic characteristics of a slave transmission gate in the flip-flop in the clock divider. Similarly, Chen et al. does not characterize inputs D, Db as being designed to substantially mimic a master output driver of the flip-flop in the clock divider. The Chen et al. reference also fails to contemplate the configuration of the output of data encoder to substantially mimic characteristics of an output driver in the flip flop.

With respect to claim 15, Chen et al. provides no teaching that would have suggested configuration of the transmission gates to correspond substantially to slave transmission gates in a flip-flop in a clock divider. Indeed, the Examiner did not provide any support for such an assertion. Similarly, Chen et al. makes no mention of a desire to configure an inverter coupled to the output of the multiplexer to correspond substantially to an output driver in the flip flop, as set forth in claim 17. The mere presence of transmission gates and an inverter in the data encoder of

Chen et al. says nothing about the manner in which they are configured, much less the specific configuration required by Applicant's claims.

The Examiner apparently intended to reject claim 21 in view of Oosera et al., and inadvertently included the discussion of claim 21 in the rejection in view of Chen et al. In any event, claim 21 is patentable over Oosera et al., for at least the reasons stated above. For example, Oosera et al. does not introduce a propagation delay that substantially matches a clock-to-Q propagation delay of the flip-flop in clock divider 11.

In general, Chen et al. simply is not directed to a delay matching circuit for matching a propagation delay introduced to a divided clock signal by a flip-flop in a clock divider. For at least this reason, Chen et al. fails to disclose or suggest the specific requirements of amended claims 14, 15, 17 and 21. Therefore, Chen et al. would not support a prima facie case of anticipation with respect to claims 14, 15, 17, and 27, or any claims dependent on those claims.

Claim Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 2, 4, 6, 7, 8, 11, 12, 22-24, 27, 29, 31, 33 under 35 U.S.C. 103(a) as being unpatentable over Oosera et al. in view of Chen et al. Applicant respectfully traverses the rejection to the extent the Examiner may consider the rejection applicable to the claims, as amended. Oosera et al. and Chen et al. fail to disclose or suggest the inventions defined by Applicant's claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention.

Claims 2, 4, 6, 12, and 29

In his analysis, with respect to claims 2, 4, 6, 12, and 29, the Examiner recognized that Oosera et al. fails to disclose several specific features of a delay matching circuit. For example, the Examiner acknowledged that Oosera et al. does not suggest a delay matching circuit having transmission gates within the multiplexer to substantially mimic characteristic of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop, as defined by claims 2 and 29.

Similarly, there is no mention in Oosera et al. of a delay matching circuit that substantially mimics output drive characteristics of the flip-flop, as in claim 4, nor a multiplexer including a select line coupled to the clock source, as in claim 6. Likewise, Oosera et al. fails to disclose means for mimicking characteristics of slave transmission gates in the flip-flop, means for mimicking characteristics of transistors in a master output driver of the flip-flop, and means for mimic characteristics of an output driver in the flip-flop, as in claim 12.

The Examiner cited Chen et al., however, as teaching such features. On this basis, the Examiner concluded that it would have been obvious to modify Oosera et al. to incorporate the features taught by Chen et al. with the somewhat cryptic motivation of "enhanc[ing] system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al."

Applicant disagrees with the Examiner's conclusion of obviousness for at least the following reasons.

First, Chen et al. does not provide the teachings attributed to it by the Examiner. As discussed above with respect to the rejection under section 102, Chen et al. makes no mention of a delay matching circuit, nor the various configurations of components within the Chen et al. circuit, to substantially mimic features of a flip-flop in a clock divider. As an example, none of the transmission gates in the Chen et al. circuit are described as being configured to substantially mimic characteristic of a slave transmission gate in a flip-flop of a clock divider. Accordingly, modification of the Oosera et al. circuit in view of the Chen et al. teachings would not result in the claimed invention.

Second, one of ordinary skill in the art would have found no reason to consult Chen et al. for modifications to the Oosera et al. circuit. For example, it is unclear why one of ordinary skill in the art, addressing problems associated with propagation delay matching, would have consulted a reference such as Chen et al., which makes no mention of propagation delay matching. The mere presence of a multiplexer or other similar circuitry in Chen et al. does not amount to a teaching that would have suggested modification of a delay matching circuit of Oosera et al. to arrive at the claimed invention.

Third, modification to include the features taught by Chen et al. would undermine the operation of the Oosera et al. circuit. If the Oosera et al. circuit were somehow modified to include a multiplexer and other components, as taught by Chen et al., it is unclear how the

resulting circuit would even be operable. The Oosera et al. circuit already provides a flip-flop in delay matching circuit 12 for the express purpose of matching the delay of the clock divider. Accordingly, Applicant is confused as to what role the Chen et al. circuitry would actually play in the Oosera et al. circuit. To the extent such circuitry would entirely supplant the Oosera et al. circuit, which already addresses the delay matching issue, then it is unclear how one of ordinary skill in the art would have considered such a modification obvious at the time of invention.

Claims 7, 8, 11, 31, and 33

With respect to claims 7, 8, 11, 31 and 33, the Examiner acknowledged that Oosera et al. fails to disclose details of a delay matching circuit including a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop, as set forth in claims 7, 8, 11, 31, and 33, or transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop, as recited in claim 8. The Examiner cited the Chen et al. reference for such a teaching, however, and asserted that it would have been obvious to modify the Oosera et al. circuit to include the features taught by Chen et al.

Chen et al. does not provide the teachings attributed to it by the Examiner. Again, Chen et al. makes no mention of a delay matching circuit, nor the various configurations of components with the Chen et al. circuit, to substantially mimic features of a flip-flop in a clock divider. Consequently, modification of the Oosera et al. circuit in view of the Chen et al. teachings would not result in the claimed invention.

In view of these basic deficiencies, Oosera et al. and Chen et al. clearly would not support a prima facie case of unpatentability. Moreover, as expressed above, Applicant questions why one of ordinary skill in the art would have looked to the teachings of Chen et al., which appear to bear no relationship to the delay matching problem, much less provide a solution to that problem.

Claims 22-24 and 27

With respect to claims 22-24 and 27, the Examiner recognized that Oosera et al. fails to disclose various details of a delay matching circuit, but again cited Chen et al. for such a

teaching. For substantially the same reasons discussed above, Applicant respectfully submits that Chen et al., which contemplates no delay matching circuit, provides no teaching that would have suggested the requisite modifications to the Oosera et al. circuit to arrive at the invention of claims 22-24 and 27. Nor would one of ordinary skill in the art have even looked to Chen et al. in contemplation of the delay matching problems addressed by Oosera et al.

CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 17-0026. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Respectfully submitted,

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